REMARKS

This Amendment is filed in response to the Office Action dated December 28, 2006, which has a shortened statutory period set to expire March 28, 2007. A two-month extension is submitted herewith, thereby allowing Applicant to respond by May 30, 2007.

Applicant Addresses 101 Rejections

Applicant has amended Claims 1, 6, 10, and 18 to clarify the invention.

Claim 1, as amended, recites:

> wherein an optimized size of the dynamic FIFO in the simulation environment determines an optimized FIFO memory size for a silicon implementation.

Claim 6, as amended, recites:

> wherein an optimized size of the dynamic FIFO in the simulation environment determines an optimized FIFO memory size for a silicon implementation.

Claim 10, as amended, recites:

> wherein decreasing the wait period and increasing the size, as needed, optimize the size and wait period of the dynamic memory, wherein an optimized size and wait period of the dynamic memory provides an actual memory size and wait period for a silicon implementation of the design.

Claim 18, as amended, recites:

> wherein an optimized combination of size and wait period of the means for storing the tokens provides an actual memory size and wait period for a silicon implementation.

Applicant respectfully submits that the recited memory size (and wait period) usable in a silicon implementation is a useful, tangible, and concrete result achieved by the claimed invention. Based on the above clarifications, Applicant respectfully requests reconsideration and withdrawal of the rejection of Claims 1, 6, 10, and 18.

Claims 2-5 depend from Claim 1, Claims 7-9 depend from Claim 6, Claims 11-17 depend from Claim 10, and Claims 19-25 depend from Claim 18. Therefore, Claims 2-5, 7-9, 11-17 and 19-25 are patentable for at least the reasons presented for Claims 1, 6, 10, and 18. Based on those reasons, Applicant also requests reconsideration and withdrawal of the rejection of Claims 2-5, 7-9, 11-17, and 19-25.

New Claims 26-50 recite comparable limitations. For example, Claim 26 recites:

> the dynamic FIFO capable of automatically increasing its size based on a configurable wait period to eliminate deadlock between the first and second units, thereby determining an optimized size of the dynamic FIFO,
>
> the dynamic FIFO including an output unit that provides the optimized size to a simulator to reduce simulation time of the first and second units.

Claim 31 recites:

> the dynamic FIFO capable of automatically increasing its size based on a configurable wait period to eliminate deadlock between the first and second units, thereby determining an optimized size of the dynamic FIFO,
>
> the dynamic FIFO including an output interface that provides the optimized size to a simulator to reduce simulation time of the first and second units.

Claim 35 recites:

> based on decreasing the wait period and increasing the size, automatically determining an optimized wait period and size and providing the optimized wait period and size to a simulator to minimize simulation time of the first and second models.

Claim 43 recites:

> means for outputting that receive outputs of the means for decreasing the wait period and the means for increasing the size, the means for outputting automatically determining an optimized combination of size and wait period of the means for storing the tokens, the means for outputting providing the optimized combination to a simulator, thereby minimizing simulation time of the first and second models.

Applicant respectfully submits that the recited optimized size and wait period that are provided to a simulator to minimize simulation time is a useful, tangible, and concrete result achieved by the claimed invention. Based on the above clarifications, Applicant respectfully requests reconsideration and withdrawal of the rejection of Claims 26, 31, 35, and 43.

Claims 27-30 depend from Claim 26, Claims 32-34 depend from Claim 31, Claims 36-42 depend from Claim 35, and Claims 44-50 depend from Claim 43. Therefore, Claims 27-30, 32-34, 36-42, and 44-50 are patentable for at least the reasons presented for Claims 26, 31, 35, and 43.

Claims 1, 4-6, And 9 Are Patentable Over Schaumont And Sevalia

Claim 1, as amended, recites:

> a dynamic first-in first-out buffer (FIFO) that interfaces between the first unit and the second unit in the simulation environment, the dynamic FIFO capable of automatically increasing its size based on a configurable wait period to eliminate deadlock, wherein an optimized size of the dynamic FIFO in the simulation environment

> determines an optimized memory size for a silicon implementation.

Applicant respectfully submits that neither Schaumont nor Sevalia disclose or suggest the recited dynamic FIFO. The First Office Action states that Schaumont fails to teach a dynamic FIFO that can increase in size. Applicant notes that Schaumont can increase the storage of a queue when the default length (16) is exceeded by put (i.e. a write operation into the queue), but only by a factor of 2. Col. 13, lines 26-29. **Notably, this doubling of storage is not based on a wait period (configurable)**. Because Schaumont cannot configure the wait period, either the final queue size of Schaumont will be quite large (i.e. significantly larger than that provided by the recited FIFO) or the whole design may crash due to size overflow.

The First Office Action cites Figures 1-8 and col. 2, lines 39-60 of Sevalia as remedying the deficiency of Schaumont. Applicant also traverses this characterization.

Sevalia teaches a multi-port FIFO with programmable width and depth that is **provided on a chip**. Col. 1, lines 6-8 and col. 5, lines 9-12. As correctly indicated by the Examiner, the **dynamic FIFO is not an actual memory circuit implemented in silicon**. As clarified by Applicant, **an optimized size of the dynamic FIFO in the simulation environment determines an optimized FIFO memory size for a silicon implementation**. Thus, the recited dynamic FIFO eliminates the need for the large block of memory (see, e.g. col. 2, lines 42-45) as well as programmability of the FIFO when it is implemented in silicon. Applicant notes that Sevalia also fails to teach anything about automatically increasing the size of the FIFO based on a configurable wait period.

Because the combination of Schaumont and Sevalia fails to disclose or suggest the recited dynamic FIFO and its advantages, Applicant requests reconsideration and withdrawal of the rejection of Claim 1.

Claims 4-5 depend from Claim 1 and therefore are patentable for at least the reasons presented for Claim 1. Based on those reasons, Applicant requests reconsideration and withdrawal of the rejection of Claims 4-5.

Claim 6, as amended, recites:

> a dynamic first-in first-out buffer (FIFO) that interfaces between the first unit and the second unit, the dynamic FIFO capable of automatically increasing its size based on a configurable wait period to eliminate deadlock between the first and second units, wherein an optimized size of the dynamic FIFO in the simulation environment determines an optimized FIFO memory size for a silicon implementation.

Therefore, Claim 6 is patentable for substantially the same reasons presented for Claim 1. Based on those reasons, Applicant respectfully requests reconsideration and withdrawal of the rejection of Claim 6.

Claim 9 depends from Claim 6 and therefore is patentable for at least the reasons presented for Claim 6. Based on those reasons, Applicant requests reconsideration and withdrawal of the rejection of Claim 9.

CONCLUSION

Claims 1-50 are pending in the present application. Allowance of these claims is respectfully requested.

If there are any questions, please telephone the undersigned at 408-451-5907 to expedite prosecution of this case.

Respectfully submitted,

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